Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 4. These sheets, which include original Figs. 1-3, 5, and 6, replace the original sheets including Figs. 1-6.

Attachment: Replacement sheets

Annotated Sheet Showing Changes

REMARKS

In response to the second non-final Office Action mailed on August 25, 2005, Applicant respectfully requests reconsideration of all objections and rejections in the outstanding Office Action in view of the foregoing amendments and following remarks. Claims 1-15 are currently pending.

I. Objection to Drawings

Fig. 4 is objected to as failing to comply with 37 C.F.R. § 1.84(o). *See* Office Action at page 2. A corrected drawing sheet of Fig. 4 in compliance with 37 C.F.R. § 1.84(o) and 1.121(d) is provided herewith. Fig. 4 as amended includes the target processor 31 mentioned in the corresponding description of this figure. Applicant believes that this amendment overcomes the objection. Accordingly, the Examiner is respectfully requested to withdraw this objection.

II. Obviousness Rejection of Claims 1-15

Claims 1-15 stand rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over U.S. Patent No. 6,199,152 to Kelly *et al.* ("Kelly") in view of U.S. Patent No. 6,631,514 to Le. *See* Office Action, page 3. Applicant respectfully traverses this rejection on the following grounds.

As stated in MPEP § 2143.01, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Kelly, either taken alone or in combination with Le, fails to teach or suggest all of the elements recited in the claims. Moreover, Kelly teaches away from making the proposed combination.

A. Kelly's Deficiencies

Following Applicant's reply of May 31, 2005, the Examiner accepts that Kelly does not teach or suggest two important features of the claimed invention:

1. Kelly does not disclose "an abstract register representing a subject register of a subject machine" as recited in step (a) of claim 1; and

2. Kelly does not disclose mapping such an abstract register to either a first location or a second location within a target machine (as recited in step (a) of claim 1) or alternating mapping of the abstract register between the first and second locations such that one represents a definitive version whilst the other represents a speculative version (as recited in step (b) of claim 1).

In other words, the Examiner accepts that Kelly does not disclose either step (a) or step (b) of claim 1.

It is worthwhile emphasizing again that Kelly is equivalent in disclosure to U.S. Patent No. 5,832,205, which is cited as background prior art on page 5, lines 13-29 of the specification. Kelly discloses an emulator that uses a set of "working" registers during emulation of each section of subject code. If the section of subject code is translated and executed successfully without generating an exception, then the "working" register values are copied to a second set of "official" registers. *See* Kelly at column 17, lines 5-10. Kelly clearly teaches that the "working" registers are always the working copy of the registers, and that the "official" registers always contain the official copy of the registers. That is, the mapping in Kelly is fixed and does not ever change.

B. Kelly Teaches Away From The Examiner's Proposed Combination

Kelly discloses an emulator combining a specially-adapted hardware processing portion (referred to as a "morph host"), working in combination with an emulating software portion (referred to as "code morphing software"). In Kelly, a register required during translation is duplicated in hardware as part of the morph host. Each required register is represented by a pair of hardware registers, one of which is permanently designated as the "official" register and the other of which is permanently designated as the "working" register. At appropriate points during translation, i.e., at the end of each section of code, the content of every "working" register is copied into the corresponding "official" register using specially adapted copying hardware (a gated store buffer). *See in particular* Kelly at column 12, line 47 to column 13, line 7.

There is no motivation for the skilled person to adapt or change the hardware-oriented code morphing system of Kelly. In contrast, Kelly teaches that copying the contents of the working register into the corresponding official register is a complete and successful solution in itself.

C. The Proposed Combination of Kelly and Le Fails to Teach or Suggest All Claim Elements

Applicant respectfully disagrees with the Examiner's suggestion that one of ordinary skill in the art at the time of the invention would combine the disclosure of Kelly with the disclosure of Le. Further, such a combination does not arrive at the claimed invention.

The Examiner draws attention particularly to column 6, line 44 to column 7, line 7 and columns 8-10 of Le. Le discloses an emulator which dynamically translates instruction code written for a first architecture into code for a second architecture. The emulator designates various check points in the original code, and speculatively re-orders the translated code instructions according to optimization procedures. If a trap (an exception) occurs during execution of the re-ordered code, then the emulator resets the original code to the most recent check point.

Applicant can find no teaching of the recited limitations of claim 1. In particular, there is no teaching in Le that an abstract register representing a subject register of a subject machine is mapped to either a first location or a second location within a target machine. Secondly, there is no teaching or disclosure in Le of alternating mapping between the first and second locations such that one represents a definitive version for use during exception handling whilst the other represents a speculative version, as recited in the claims.

Le is quite different to the claimed invention. Le discloses that a register R_x in executable object code for a legacy instruction set architecture is mapped using a register map (RMAP) to a corresponding native register r_x. There is a one-to-one initial mapping from the legacy register R_x to its corresponding physical architectural register r_x. Figure 2C of Le shows that in order to take advantage of instruction level parallelism (ILP) in the native system, the emulator/translator uses register re-naming to break all write after read (WAR) and write after write (WAW) register dependencies, allowing loads and most other operations to be scheduled speculatively. These temporary results are stored in additional temporary registers, on the assumption that the native system has a greater number of registers than the legacy architecture.

Every time a register is renamed, the current RMAP entry is saved and then associated with a particular instruction. If an exception (a trap) occurs then the translator reverts back to the most recent checkpoint for this section of code, using the register state defined by the check point's RMAP. The translator then proceeds as if the optimization had never taken place.

Notably, Le essentially employs register re-naming. By updating the register map (RMAP), there is always an exact one-to-one relationship between a register R_x of the legacy architecture and exactly one valid register in the native target architecture.

Secondly, there is also absolutely no teaching or suggestion in Le of alternating mapping such that the roles of the first and second locations are reversed, whereby one of those first or second locations holds the definitive version of the abstract register, whilst the other represents a speculative version of the abstract register. In the present invention, there will be times when the first location is definitive whilst the second location is speculative. Equally, due to the step of "alternating mapping," there will be times when the second location is definitive whilst the first location is speculative.

In summary, Kelly and Le teach in quite different directions. Kelly teaches a fixed mapping with a gated store buffer in hardware to copy between a working register and an official register. Le teaches register re-naming and storing register maps (RMAPs) associated with particular instructions. In combination the documents still fail to disclose the claimed invention.

Hence, Le fails to cure Kelly's deficiencies noted above with respect to independent claim 1. Independent claims 9 and 12-15 are nonobvious for at least the same reasoning. Dependent claims 2-8, 10, and 11 are nonobvious at least because they depend from either independent claim 1 or claim 9.

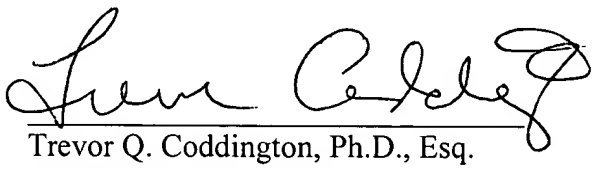
Applicant respectfully requests the Examiner to withdraw this prior art rejection.

III. Conclusion

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

Applicant is concurrently filing herewith a Petition for a One-Month Extension of Time, along with the requisite fee. In the event that a variance exists between the amount tendered and that required by the U.S. Patent and Trademark Office requires to enter and consider this Reply, or to prevent abandonment of the present application, please charge or credit such variance to the undersigned's Deposit Account No. 50-2613 (Order No. 45256.00005.CIP1).

Respectfully submitted,

December 22, 2005 By: 

Trevor Q. Coddington, Ph.D., Esq.
Registration No. 46,633

PAUL, HASTINGS, JANOFSKY & WALKER LLP
Customer Number: 36183
P.O. Box 919092
San Diego, CA 92191-9092
Telephone: (858) 720-2500
Facsimile: (858) 720-2555

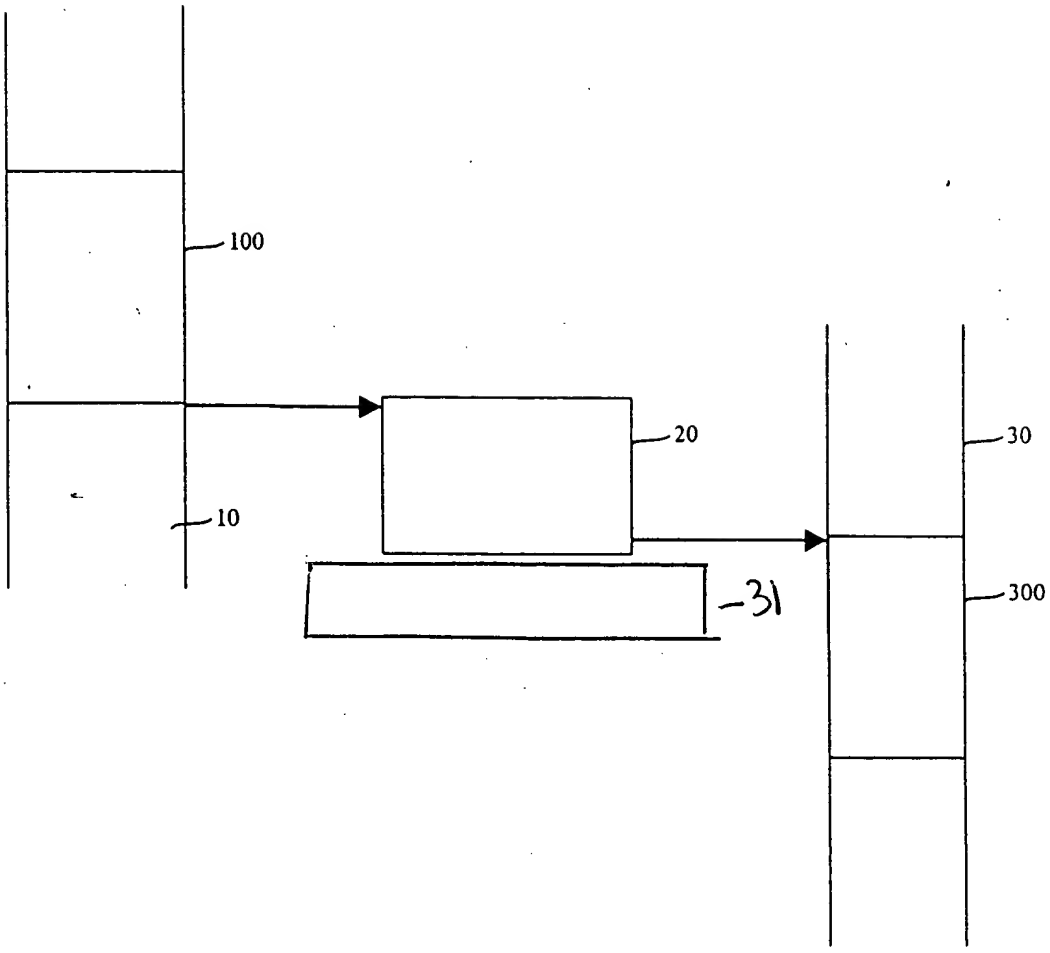


Fig. 4